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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,482	09/27/2004	Pieter Jan Van Der Zaag	GB02 0030 US	5415

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
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EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/509,482	VAN DER ZAAG ET AL.	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09-27-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 09-27-2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because total word count exceeds 150.

Correction is required. See MPEP § 608.01(b).

Response to Amendment

5. **Status:** Receipt is acknowledged of papers submitted on September 27, 2004 under amendments, which have been placed of record in the file. Claims 1-16 are pending in this

action. The amendment filed 09-27-2004 does not introduces new matter into the disclosure. Applicant has merely changed dependency of the dependent claims. The added material, which is supported by the original disclosure. Please all the replies and correspondence should be addressed to examiner's new art unit 2629.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1,and 2 rejected under 35 U.S.C. 102(e) as being anticiapted by Daughton et al. (US 6,538,921 B1).

Regarding Claim 1, Daughton et al. teaches a memory circuit (Col. 5, Lines 55) comprising: one or more magnetoresistive random access memories (page 6, Lines 31-34), MRAMs (Col. 6, Lines 31-40), coupled to a flip-flop circuit (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73).

Regarding Claim 2, Daughton et al. teaches two MRAMs and the flip-flop circuit, the flip-flop circuit comprising two inputs, each of the two MRAMs being coupled to a respective

one of the flip-flop circuit inputs (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daughton et al. (US 6,538,921 B1) as applied to claims 1 and 2 above, and further in view of Toyota et al. (US 2006/0216877 A1).

Regarding Claims 3-16, Daughton et al. teaches two MRAMs and the flip-flop circuit, the flip-flop circuit comprising two inputs, each of the two MRAMs being coupled to a respective one of the flip-flop circuit inputs (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73) and the bit line passes over the first MRAM then turns or meanders back on itself before passing over the second MRAM (Col. 23, Lines 16-51, and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73) and a MRAM memory circuit further comprises a flip-flop circuit (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73); and the bit line being arranged to cross over the first MRAM in a first direction and to cross over the second MRAM in a second direction, the first direction being

substantially opposed to the second direction (Col. 23, Lines 16-19, Line 34-42 and Col. 6, Lines 31-40, also see figures 2,6,10 Items 21, 62-73).

However, Daughton et al. fails to teach specific display application where each pixel of a display is being associated with a respective one of the memory circuits and forms in-pixel memory.

However, Toyota et al. teaches each pixel being associated with a respective one of the memory circuits (pages 7 and 8, paragraph 92 figure 28, items 221,22 and 230, page 9, paragraph 110); a pixel and memory assembly for a display device, comprising: a pixel display electrode coupled to in-pixel memory means, the in-pixel memory means comprising one or more MRAMs (pages 7 and 8, paragraph 92 figure 28, items 221,22 and 230, page 9, paragraph 110); a pixel and in-pixel memory for a display device, comprising: a switching device; a pixel electrode; a first MRAM; a second MRAM; and a bit line, the bit line running from the switching device to the pixel electrode (pages 7 and 8, paragraph 92, see figure 28, items 221,22 and 230, page 9, paragraph 110); the bit line connects with a respective one end of each of the first and second MRAMs; and further comprising: a word line, running under the other ends of each of the first and second MRAMs, for addressing the MRAMs; and a gate line, for driving the switching device, coupled to the switching device; the word line being arranged between the pixel electrode and the gate line such that the bit line passes over the word line but does not pass over the gate line (pages 7 and 8, paragraph 92, figure 28, items 221,22 and 230, page 9, paragraph 110 and page 8, paragraphs 93,94, page 7, paragraphs 85-91); a pixel and in-pixel memory for a display device (pages 7 and 8, paragraph 92), comprising: a switching device; a pixel electrode; one or more MRAMs (pages 7 and 8, paragraph 92 figure 28, items 221,22 and

230, page 9, paragraph 110); a bit line running from the switching device to the pixel electrode via one end of each of the one or more MRAMs (pages 7 and 8, paragraph 92, page 8, paragraphs 93,94, figure 28, items 221,22 and 230, page 9, paragraph 110, page 7, paragraphs 85-91); and a gate line, for driving the switching device, coupled to the switching device; the word line being arranged between the pixel electrode and the gate line such that the bit line passes over the word line but does not pass over the gate line (pages 7 and 8, paragraph 92 figure 28, items 221,22 and 230, page 9, paragraph 110 and page 8, paragraphs 93,94, page 7, paragraphs 85-91); a word line, running under the other ends of each of the one or more MRAMs, for addressing the MRAMs (page 7, paragraphs 85-91); a display device comprising a pixel and in-pixel memory with active matrix elements and drive lines of the display device (pages 7 and 8, paragraph 92, see figure 28, items 221,22 and 230, page 9, paragraph 110); a method of forming an in-pixel memory display device, forming a switching device; forming an in-pixel memory circuit comprising one or more MRAMs coupled to a read-out circuit (pages 7 and 8, paragraph 92, see figure 28, items 221,22 and 230, page 9, paragraph 110); forming a word line, for addressing the in-pixel memory circuit; and forming a gate line, for driving the switching device; wherein the word line and the gate line are formed during a same masking stage (page 5, paragraph 68, figure 14D); forming a switching device and forming an in-pixel memory circuit comprising one or more MRAMs coupled to a read-out circuit; forming a bit line, for addressing the in-pixel memory circuit; and forming a column line, for driving the switching device (pages 7 and 8, paragraph 92 figure 28, items 221,22 and 230, page 9, paragraph 110 and page 8, paragraphs 93,94, page 7, paragraphs 85-91); wherein the bit line and the column line are formed during a same masking stage (page 5, paragraph 68, figure 14D);

forming a word line, for addressing the in-pixel memory circuit; and forming a gate line, for driving the switching device; wherein the word line and the gate line are formed during a further same masking stage (page 5, paragraph 65-71, figure 14D, page 7, paragraphs 85-91, page 4, paragraph 57, page 3, paragraph 51) and the in-pixel MRAM memory circuit pages 7 and 8, paragraph 92, figure 28, items 221,22 and 230).

The reason to combine Daughton et al. teaches Such memories can be advantageously based on the storage of digital symbols as alternative states of magnetization in magnetic materials provided in each memory storage cell, the result being memories which use less electrical power and do not lose information upon removals of such electrical power. a memory circuit comprising: magnetoresistive random access memories MRAMs, but fails to teach a specific application such as display where a pixel structure of display is associated with MRAM where power consumption is major concerned.

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Toyota et al. to the teaching of Daughton et al. to be able to have a display system where a pixel structure of display is associated with MRAM which use less electrical power and do not lose information upon removals of such electrical power.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Touminen et al. (US 2002/0158342 A1) Nanofabrication.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

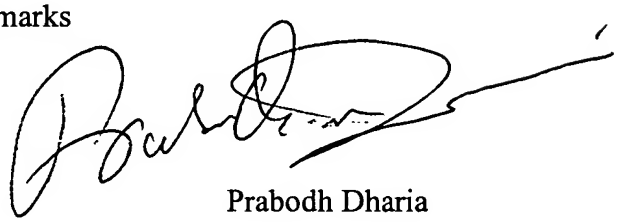
12. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231



Prabodh Dharia

Partial Signatory Authority Program

AU 2629

November 10, 2006